30 Gb/s All-Optical Clock Recovery Circuit

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***Abstract*—All-optical clock recovery is demonstrated from pseudo-data patterns at 30 Gb/s. The circuit is based on the optical gain modulation of a semiconductor optical amplifier fiber laser. The recovered clock is a 2.7-ps pulse train, with very low modulation pattern even in the presence of more than 200 consecutive 0's in the data signal.**

***Index Terms*—All optical, clock recovery, ring laser, semiconductor optical amplifier.**

I. Introduction

In the recent past, there has been an intense effort in the demonstration and deployment of very high capacity WDM/TDM network transmission systems and ultrahigh-speed all-optical digital logic circuits [1], [2]. In order to ensure data synchronization in these applications, it is of crucial importance to be able to generate a high quality local clock in the presence of jittered signal. Optical clock recovery circuits that use phase modulation in an optical fiber in an EDFA ring laser [3] and the nonlinear dynamics of a NOLM in a figure eight laser [4], [5] have been demonstrated. Injection mode-locked laser diodes [6], [7] and self-pulsating two-section DFB laser diodes [8] have also been used to recover clock.

In this letter, we demonstrate a simple clock recovery circuit based on a fiber ring laser, which contains a single semiconductor optical amplifier (SOA) as active device and which provides both gain and modulation. The circuit was tested with both pseudorandom data sequences from a bit-error-rate test set (BERT) and periodic data patterns with very long sequences of consecutive 0's. The circuit has been operated up to 30 Gb/s and can generate clock pulse trains of 2.7 ps across a 20 nm tuning range, with very low pattern despite the long series of consecutive 0's. It has also been shown that a second SOA may be added at the output of the circuit, to remove any remaining modulation pattern on the recovered clock. The operation of the present clock recovery circuit relies on the fast gain saturation of the SOA by the incoming data stream. The gain saturation of the SOA results in modulation in the cavity and mode-locks the fiber laser.

Mode-locking of a SOA fiber ring laser with a CW optical pulse train has been demonstrated before up to 40 GHz [9], but here the technique is extended to a modulated data stream. Desirable features of this clock recovery circuit are the wide repetition frequency and wavelength ranges of incoming data over which it locks, and the broad wavelength tuning range of recovered signal that it may provide. Furthermore the circuit is nearly polarization insensitive and is simple to build from commercially available components.

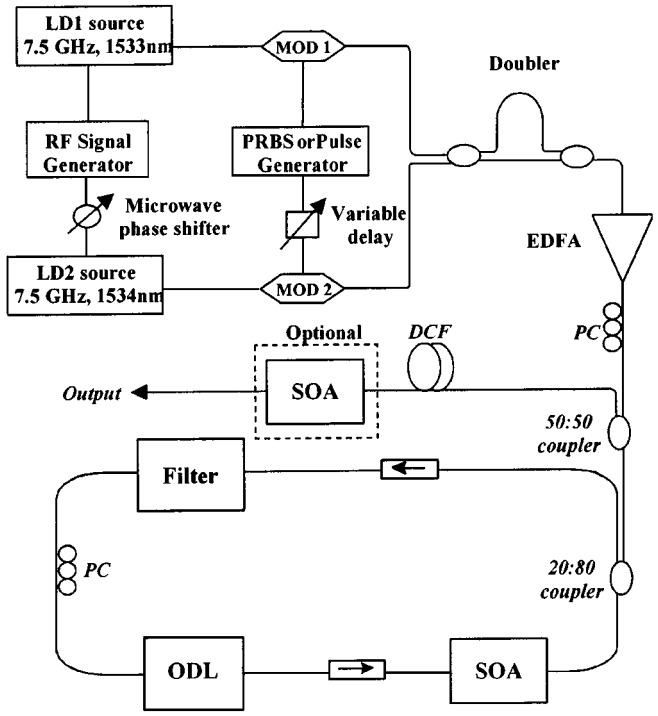

Fig. 1. Experimental layout of clock recovery circuit.

II. Experiment

Fig. 1 shows the experimental layout. The cavity of the clock recovery circuit was constructed entirely from fiber-pigtailed devices. Gain was provided from a 500-μm bulk InGaAsP–InP ridge waveguide SOA. The SOA had a peak gain at 1535 nm and could provide 23-dB small-signal gain with 250-mA dc drive current.

The SOA exhibited 2-dB polarization gain dependence and a polarization controller was used at its input for performance optimization. Faraday isolators were used at the input and output of the SOA to ensure unidirectional oscillation in the ring. The incoming data pattern and recovered clock signal were introduced in and extracted from the circuit with a 20 : 80 fused optical fiber coupler. A 5-nm tunable optical filter was used for wavelength selection and a variable optical delay line (ODL) was used for precise matching of the repetition frequency of the clock recovery circuit to the incoming data pattern. The total linear loss of the cavity was 10 dB and its fundamental frequency was 7.44 MHz.

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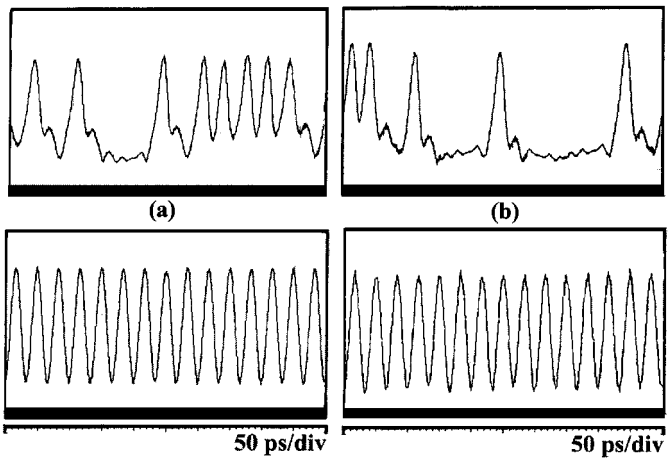

Fig. 2. Data pattern (upper row) and recovered clock (lower row) for (a) $2^{10}-1$ and (b) $2^{15}-1$ PRBS data sequences.

The test data patterns were produced using two DFB laser diodes gain switched from a common signal generator up to 7.5 GHz and which operate at 1533 and 1534 nm. The pulse trains from the two diodes were subsequently linearly compressed to 7 ps with dispersion compensation fiber (DCF) of total dispersion of -34.4 ps/nm. The compressed pulse trains were modulated in lithium niobate modulators, driven from the synchronized channels of a BERT pattern generator or a programmable pulse generator. The patterns from each diode were bit interleaved to 15 Gb/s and repetition frequency doubled to 30 Gb/s using a split-relatively-delay-and-recombine fiber doubler. Use of this flexible test data pattern generator has allowed testing of the clock recovery circuit at 7.5, 15, and 30 Gb/s, both using the pseudorandom data pattern from the BERT set and patterns with very long series of consecutive 0's from the programmable pulse generator. The modulated data pattern was amplified in an EDFA capable of delivering up to 1 mW average power into the clock recovery circuit. The polarization state of the input pattern was adjusted with a controller before introduction into the ring for optimum performance.

III. Results and Discussion

With the ODL adjusted so that the fundamental frequency of the fiber ring is a harmonic of the line frequency of the data pattern, the clock recovery circuit generates mode-locked pulse trains. The output pulses were monitored on a second harmonic autocorrelator and found to be 6 ps long and not transform limited.

These pulses were next compressed to 2.5 ps with DCF of -14.25 ps/nm total dispersion. The pulsewidth-bandwidth product of the compressed pulses was 0.34, very close to that of a squared hyperbolic secant profile. Fig. 2(a) and (b) shows samples of the PRBS data sequences with length $2^{10}-1, 2^{15}-1$, respectively, (upper row) and the recovered clock (lower row), showing negligible output modulation pattern. The recovered clock was also monitored on a 40 GHz microwave spectrum analyzer and revealed suppression of the clock rate subharmonics in excess of 40 dB with respect to the recovered clock signal.

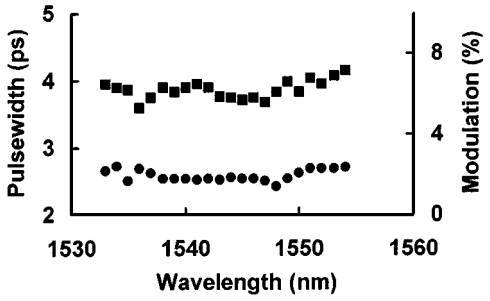

Fig. 3. Pulsewidth (•) and output modulation pattern (■) against wavelength for the 30 GHz recovered clock with $2^{15}-1$ input PRBS.

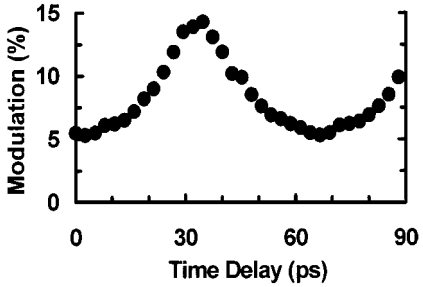

Fig. 4. Modulation pattern variation against relative delay between the two time interleaved 15 Gb/s PRBS sequences.

The fast gain dynamics of the SOA in the clock recovery circuit gives rise to a clock recovered signal that displays a low pattern following roughly the modulation pattern of the incoming data stream. In order to quantify this pattern, we use as its measure the ratio $(P_p^{\max}-P_p^{\min})/(P_p^{\max}+P_p^{\min})$. Fig. 3 shows the variation of the modulation pattern on the recovered clock signal for a $2^{15}-1$ PRBS data pattern at 30 Gb/s, across the tuning range of the circuit. Fig. 3 also displays the variation of pulse width of the recovered signal with wavelength. The circuit generates nearly transform-limited pulses, which are within 6% of 2.7 ps across a 20-nm tuning range. The modulation pattern on the signal directly out of the clock recovery circuit is less than 8% and is nearly constant across the tuning range. The output power from the circuit was within 7% of 70 μW across its tuning range. Long scan autocorrelations of the extracted pulse train have shown that the pulse to pulse jitter was less than 400 fs. The circuit was also tested with 7.5- and 15-Gb/s test patterns and produced quantitatively similar results.

The effect of mistiming between the two 15-Gb/s PRBS data patterns from the two diodes, was also investigated in order to evaluate performance degradation as the incoming bits deviate from their expected arrival time. Timing jitter appears as a statistical variation in the arrival time of each bit around its predetermined arrival time. Our investigation does not include this statistical variation, but it allows the evaluation of performance degradation up to the maximal mistiming between two consecutive bits of up to one full bit period. It was found that the circuit always recovers clock at 30 GHz albeit with an increased modulation, even if the two patterns are mistimed by one full bit period. In this case and as the clock recovery cavity is tuned for 30 GHz oscillation, it operates as to multiply the repetition frequency of the incoming data by a factor of 2 [10]. Fig. 4 shows

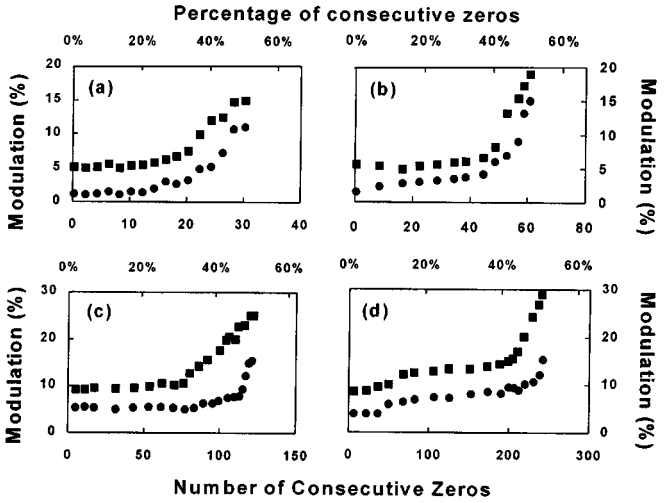

Fig. 5. Output modulation pattern variation in 30 GHz recovered clock as the number of consecutive zeros changes, directly from circuit (■) and with the addition of a second SOA (•) at its output. (a) 500 MHz, (b) 250 MHz, (c) 125 MHz, and (d) 62.5 MHz

the variation of the recovered clock pattern as the relative delay between the two patterns is varied.

In order to determine the penalty on the recovered clock signal for very long series of consecutive 0's as may happen in real data traffic, the lithium niobate modulators generating the data pattern were driven with a two-channel programmable pulse generator. This penalty is expected to manifest itself in the form of the modulation pattern on the recovered clock. The modulators were driven at different rates and duty factors corresponding to varying numbers of consecutive 0's. As the use of the SOA in the clock recovery circuit results in a pattern effect due to its fast gain dynamics, a second SOA may be employed on its output to reduce this pattern further. The SOA at the output of the clock recovery circuit is operated around its saturation point so that its gain saturation leads to a reduction of the modulation at the output of the clock recovery circuit. Fig. 5 shows the modulation pattern for (a) 500 MHz, (b) 250 MHz, (c) 125 MHz, and (d) 62.5 MHz pattern repetition rates, directly from the clock recovery circuit and with the use of the additional SOA as the number of consecutive 0's is increased. The figure is also labeled in terms of the percentage of consecutive 0's in each test data pattern. This figure shows that even with 212 (or 44%) of the bits in the pattern being consecutive 0's, the clock recovery circuit provides signal with less that 15% modulation pattern. It should be noted that 212 consecutive 0's is a highly unlikely occurrence for a data pattern in a transmission environment.

The same figure also shows a drastic improvement of the modulation pattern with the use of the additional SOA at the output of the clock recovery circuit. For 212 consecutive 0's the pattern drops to less than 9%. The addition of the second SOA would indeed increase the complexity and cost of this clock recovery circuit. It should be noted however that a practical clock recovery circuit used in an optical system, would require an amplifier at its output to drive the following stages after it. In this sense the additional SOA would replace an EDF amplifier that would normally be used, with the added benefit of significantly improving its performance.

IV. Conclusion

We have demonstrated a simple and robust clock recovery circuit suitable for use in high-speed, transmission, and digital all-optical logic circuits. The circuit has been evaluated up to 30 Gb/s and has been shown to produce stable, nearly transform limited pulse trains of 2.7-ps duration width, across a 20 nm tuning range circuit. The data repetition frequency at which the circuit operates is limited by the gain and recovery time of the SOA. As the fiber ring laser has already been operated to 40 GHz [9], it is expected that this clock recovery circuit would be capable of at least this speed without changes in the SOA. The circuit has been exhaustively characterized and the quality of the recovered clock has been investigated for data patterns with different compositions of "0's" and "1's." It has been shown that the circuit produces clock signal with low modulation pattern even in extreme cases of long sequences of consecutive 0's. It has also been shown that the use of a second SOA at the output of the circuit may reduce the modulation pattern even further.

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