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Optical clock recovery and clock division at 20 Gb/s using a tunable semiconductor fiber ring laser

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Abstract

Optical clock recovery and clock division is demonstrated from a pseudo-data pattern at 20 Gb/s, using a semiconductor optical amplifier fibre ring laser. The ring laser is capable of generating 4.7 ps pulses at 20 GHz repetition rate and less than 3 ps pulses at the divided clock frequencies of 10 and 5 GHz, over a 16 nm tuning range. The effect of the input data pattern on the recovered clock signal is investigated. The extinction ratio of the recovered clock signal to the clock sub-harmonics was found to be as high as 40 dB despite the long series of consecutive zeros of input pattern.

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Keywords: All optical; Clock recovery; Clock division; Semiconductor optical amplifier; Fiber ring laser

1. Introduction

During the past years, there has been intense effort in the design and demonstration of high speed, all-optical processing systems using semiconductor-based, fiber or integrated circuits [1,2]. One of the key support functions necessary to make these circuits practically realizable, is the ability to generate locally a reference clock signal from the incoming data stream either at the line rate or at a sub-multiple. Clock extraction at the data rate is important in order to implement all-optical regenerators, to perform data recovery or to achieve synchronization in remote optical pro-

cessing units. Similarly, sub-harmonic clock extraction is also important for down-grading the line rate in optical processing units, which must operate at a lower speed, as for example in demultiplexing circuits. So far a number of clock recovery designs have been demonstrated, using mode-locked EDFA or semiconductor ring lasers [3–5], electronic phase-lock loops [6], self-pulsating lasers [7] or mode-locked semiconductor lasers [8,9]. In addition, for sub-harmonic clock recovery, a number of circuits have been used up to date including SOA-based nonlinear loop mirrors [10], mode-locked semiconductor lasers [11] or a SOA/grating filter switch [12].

In the present communication we demonstrate clock division and clock recovery using a single circuit at 20 Gb/s. The circuit is based on a semiconductor fiber ring laser that uses a single SOA

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device to provide gain and gain modulation in the cavity. The circuit has been used for optical pulsetrain generation at repetition rates up to 40 GHz [13] as well as for clock recovery up to 30 Gb/s [5]. However, all-optical clock division is a much more difficult task and has never before been demonstrated with a mode-locked semiconductor fiber ring laser. The technique here is similar to sub-harmonic clock extraction using mode-locked semiconductor lasers [8,9,11]. However, the use of a semiconductor-based ring laser offers significant performance and operational advantages. For example the same circuit can be used either for clock recovery at the line rate or at any of the sub-multiple of the line rate, since it is a tunable oscillator that can be adjusted to oscillate and mode-lock at a frequency defined by the cavity length. Moreover, the use of a single active element in the cavity results in stable operation against environmental perturbations, like thermal fluctuations or acoustic vibrations. This is mainly due to the short cavity length as a result of not using EDFA for amplification and not using polarization sensitive components like amplitude modulators. Furthermore, the use of gain modulation as opposed to loss modulation that the majority of ring lasers use to achieve mode-locking, results in no pulsetrain loss even in the presence of long series of continuous '0' in the incoming data stream. Finally a significant performance advantage is its wavelength tunability due to the broad gain profile of the SOA. In the present experiment, the clock division/recovery circuit seems to possess a 16-nm tuning range across which output power and pulselwidth of the sub-harmonic or line-rate extracted clock is constant. This is a significant feature, since it allows the use of the same circuit for a number of wavelength-channels with no modification.

Using this semiconductor fiber ring laser, we demonstrate clock extraction and sub-harmonic clock extraction by a factor of 2 and 4 from a 20 Gb/s data signal. The ring laser is capable of providing less than 4.7 ps pulsetrains either at 5, 10 or 20 GHz repetition rate with an average output power of 0.3 mW. The recovered clock signal has been investigated for a number of data input streams with particular emphasis in long series of

consecutive zeros. The goal was to test the ability of the circuit to recover a clock signal either at the line rate or at a sub-rate, from various input patterns independently of their frequency content.

2. Experimental set-up

The basic concept on which the clock recovery/division circuit operates relies on the fast gain saturation and slow recovery of the intracavity SOA by external optical pulses and which has been recently used to mode-lock a SOA fiber ring laser up to 40 GHz [13]. Fig. 1 shows the experimental layout. The clock recovery/division circuit was constructed entirely from fiber-pigtailed devices. Gain was provided from a 500 μ m, bulk Semiconductor Optical Amplifier. The SOA had a peak gain at 1535 nm and could provide 23 dB small signal gain with 250 mA dc drive current. Faraday isolators were used at the input and output of the

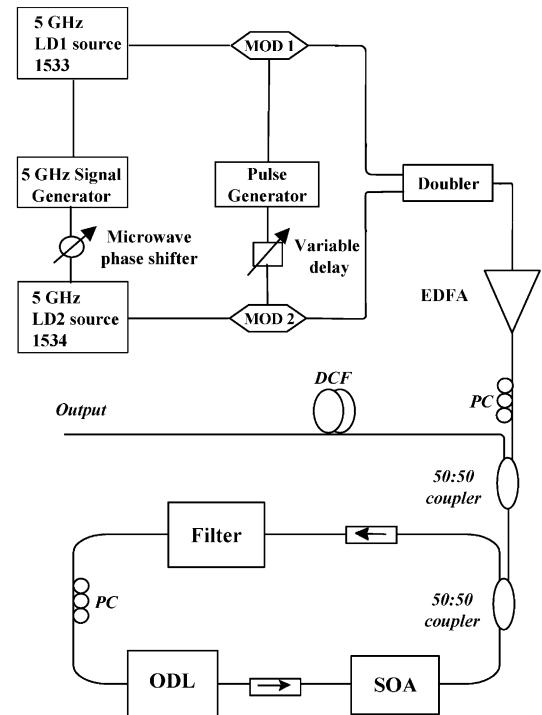


Fig. 1. Experimental set-up of the clock recovery/division circuit.

SOA to ensure unidirectional oscillation in the cavity. A 4.8 nm tunable optical filter was used for wavelength selection and a variable optical delay line (ODL) for precise tuning of the repetition frequency of the circuit to the incoming data pattern. As the SOA exhibited a 2 dB polarization gain dependence, a polarization controller was introduced at its input port. After the SOA, a 3 dB fused optical fiber coupler was positioned to insert the external modulating signal and to obtain the output from the source. The externally introduced programmable data sequence, was constructed using two 5 GHz gain switched DFB laser operating at 1533 and 1534 nm and driven from a common signal generator with the addition of a variable phase shifter on one of the two. The output of each DFB was externally compressed with dispersion compensating fiber of total dispersion -47.5 ps/nm, to produce 12 ps pulses. These pulses were modulated in lithium niobate modulators, driven from the two synchronized channels of a programmable 500 MHz pattern generator at selectable rates and duty factors to obtain various data sequences. In particular the two modulators were driven at 500, 250, 125 and 62.5 MHz with various duty cycles. In this case, at the modulators outputs two *synchronous packet streams* were formed containing only '1s', and which streams were interleaved in the following fiber doubler to form a 20 Gb/s pseudo-data pattern. Depending on the branch delay of the split, relative delay and recombine fiber doubler as well as on the delay imposed on the electrical modulating signals (using the microwave phase shifter and the electrical delay line) various optical data streams could be obtained, with frequency components at 5, 10 and 20 GHz. To this end, it was possible to test the capability of the circuit to perform either clock division at 5 or 10 GHz or to perform clock recovery at 20 GHz and to measure the minimum required power level of the frequency components. It is worth noticing here that for sub-harmonic clock recovery, it is essential to keep even a weak sub-harmonic frequency component in the incoming data signal, since this component forces the cavity to mode-lock at this frequency. This is especially important for optical networks that use OTDM to generate a high-speed

optical channel by multiplexing many independent lower rate channels. To this end, clock division circuits are of paramount importance for extracting a sub-line rate clock signal for the demultiplexing of the independent lower rate channels. In our experiment we retained a 5 GHz (or 10 GHz) frequency component at least -32 dB lower than the power level of the 20 Gb/s data signal.

The generated 20 Gb/s data stream was then amplified in an EDFA and launched into the clock recovery/division circuit. In real network applications, the EDFA can be omitted if the power level of the incoming data stream is optimized across the transmission link to fit in a certain input power range of the clock recovery/division circuit.

3. Results and discussion

With the EDFA adjusted to provide around 300–600 μ W, into the ring cavity and the ODL adjusted, the clock recovery breaks in mode-locked operation. Within this input power range, optimum operation has been achieved for power levels close to 400 μ W. Fig. 2 show two samples of the incoming data patterns with different contents of '1s' and '0s' and the respective clock output from the circuit at 20, 10 and 5 GHz, monitored on a 40 GHz sampling oscilloscope. More specifically, Figs. 2(a) and (e) show the incoming pseudo-data patterns, while Figs. 2(b), (c), (d) and Figs. 2(f), (g), (h) display the corresponding 20, 10 and 5 GHz recovered clock. In the case of sub-harmonic clock recovery the cavity length was adjusted so that the circuit to oscillate at 10 or 5 GHz. The output pulses were not transform-limited due to the frequency chirp imposed by the time-dependent refractive index change of the SOA. To this end, 4.7 ps pulses were obtained at 20 GHz and less than 3 ps at 5 and 10 GHz, after linear compression with -11.4 ps/nm dispersion compensating fiber.

The input data pattern and output signal from the circuit were also monitored on an RF spectrum analyzer. The RF spectrum of the input data pattern contained modes at 5, 10, 15 and 20 GHz, while the output signal from the circuit contained only one strong component either at 20,

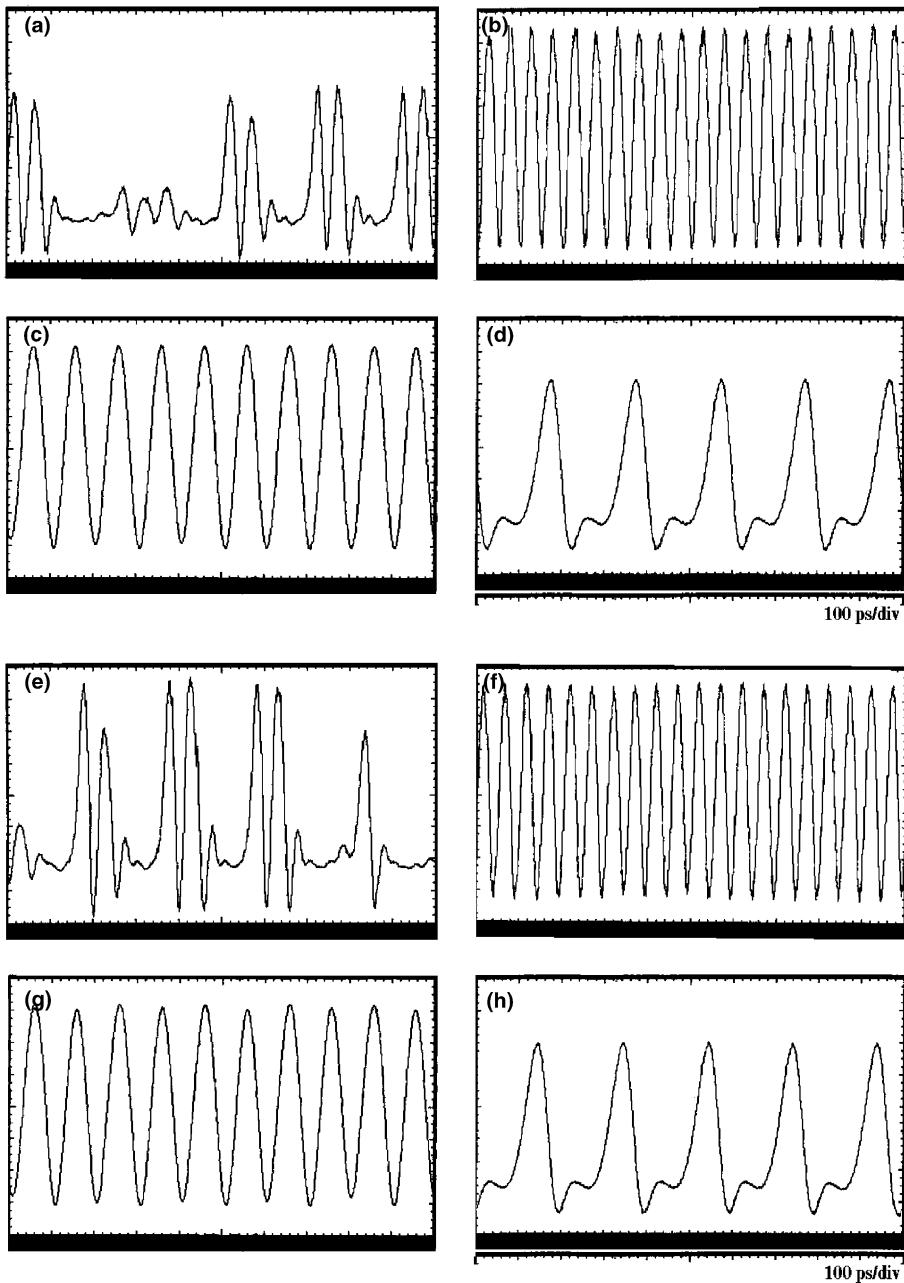


Fig. 2. (a) and (e) Temporal samples of the input data sequence, (b) and (f) corresponding 20 GHz recovered clock, (c) and (g) corresponding 10 GHz recovered clock, (d) and (h) corresponding 5 GHz recovered clock. The timebase is 100 ps/div.

10 or 5 GHz and very weak contributions from the rest frequencies. We measured the power of the various frequency components of the output signal and compare it with the corresponding ones in the

input. In particular, we investigated the minimum required power level in order to achieve sub-harmonic clock recovery at 10 and 5 GHz and furthermore we measure the frequency suppression

ratio at the output. Fig. 3 shows the case of 10 GHz sub-harmonic clock recovery. More specifically, it shows the (■) 10-to-20 GHz extinction ratio in the output signal versus the same ratio in the input data stream. From this curve, it can be seen that the enhancement of the 10 GHz over the 20 GHz component is, in most cases, more than 63 dB, while the worst-case suppression ratio in the output signal was found to be more than 30 dB. It is worth noticing that for clock division by a factor of 2 from 20 Gb/s data, a minimum power level of -32 dB of the 10 GHz component against the 20 GHz component must be retained in order to obtain an 10 GHz output signal with an extinction ratio in excess of 35dB. Fig. 3 also shows the (●) 10–15 GHz and the (▲) 10-to-5 GHz excess power in the output signal. It can be seen that these components are highly suppressed at the output and their extinction ratio exceeds on average 35 dB, while in some cases it exceeds 40 dB.

A similar set of measurements were also performed in the case of 5 GHz sub-harmonic clock extraction. Fig. 4 shows the corresponding results, from which it can be seen, that a minimum power level of -34 dB of the 5 GHz component must be retained in the input data stream in order to achieve a frequency suppression of more than 35 dB in the 5 GHz output signal. Fig. 4 also shows the suppression ratio of the (●) 15 GHz and (▲) 10 GHz component in the output signal, which

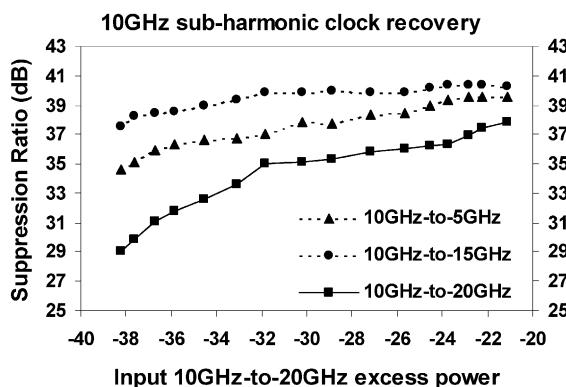


Fig. 3. 10 GHz sub-harmonic clock extraction. (■) 10-to-20 GHz extinction ratio in the output signal versus the same ratio in the input data stream. Corresponding (●) 15 GHz and (▲) 5 GHz suppression ratio in the output signal.

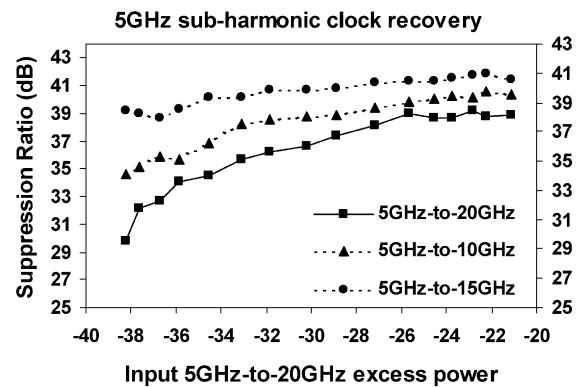


Fig. 4. 5 GHz sub-harmonic clock extraction. (■) 5-to-20 GHz extinction ratio in the output signal versus the same ratio in the input data stream. Corresponding (●) 15 GHz and (▲) 5 GHz suppression ratio in the output signal.

in most cases exceeded 37 dB, independently of the power level of the 5 GHz frequency component in the input stream.

To conclude the RF measurements, we have also measured the frequency suppression ratio in the case of line-rate clock recovery from pattern samples with different numbers of '0s'. Fig. 5 shows the excess power of the 20 GHz component over the (a) 5 GHz, (b) 10 GHz and (c) the 15 GHz component, in the input (▲) and output (■) signals, as a function of the percentage of consecutive '0s' in the input pattern. The extinction of the sub-harmonics in the recovered clock is in excess of 30 dB for the different patterns tested and in some cases exceeded 40 dB. From Fig. 5, it can be seen that the clock recovery circuit is capable of recovering a high quality clock signal even in the case of 40% consecutive '0s' in the incoming data.

Analysis of the spectrum at the output of the source using inverse Fourier series indicates that the amplitude modulation of the signal is below 0.20 dB, which agrees well with the measurements made with the sampling oscilloscope. Spectral analysis has also shown that the timing jitter was less than 500 fs. The timing and the amplitude jitter of the divided clocks was also measured and was found to be close to 480 fs and 0.12 dB for the 5 GHz divided clock and 500 fs, 0.21 dB for the 10 GHz divided clock.

It is worth noticing that because of the broad gain spectrum of the SOA, the circuit exhibits a

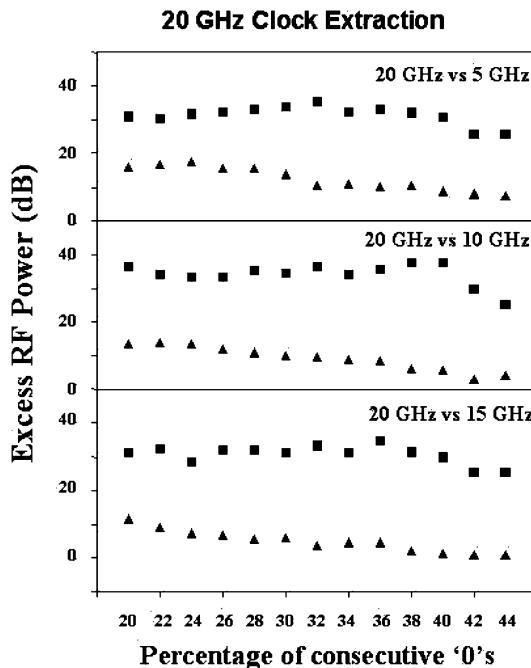


Fig. 5. 20 GHz clock extraction. Excess power of 20 GHz signal over the 5, 10 and 15 GHz subharmonics for the (▲) input and (■) output data stream against the percentage of the consecutive '0's' in the input data stream.

broad tuning range. Figs. 6 and 7 show the change of the pulse width and the average optical power respectively of the recovered clock signal versus wavelength when the circuit was tuned to operate either at 20, 10 or 5 GHz. From Fig. 6, it can be seen that the circuit is capable of generating 4.7 ps

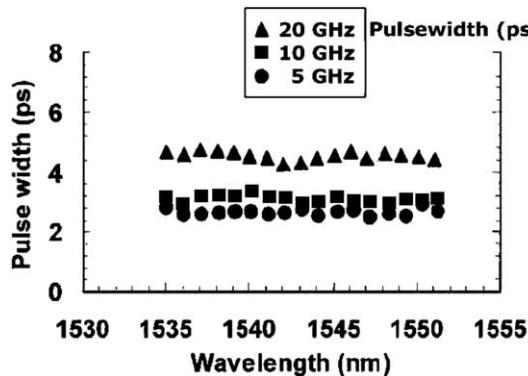


Fig. 6. Tuning curves for pulse width of the recovered clock pulses at 20, 10 and 5 GHz repetition rate.

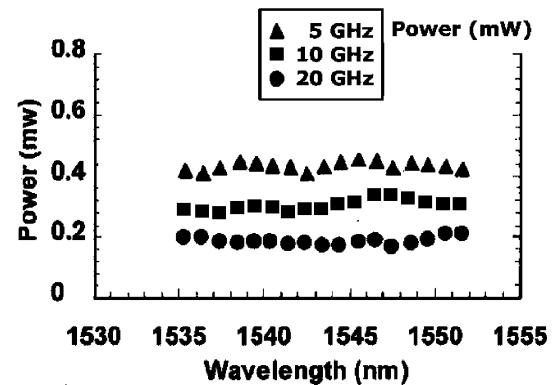


Fig. 7. Tuning curves for average power of the recovered clock pulses at 20, 10 and 5 GHz repetition rate.

pulses at 20 GHz repetition rate and less than 3 ps at 10 and 5 GHz. In addition the average output power was close to 200, 300 and 400 μ W at 20, 10 and 5 GHz, respectively. Both the pulsewidth and output power is nearly constant across a 16 nm tuning range for all the operating frequencies. The tuning curves were obtained easily, and both polarization controllers were necessary only for detailed optimization.

4. Conclusions

In summary we have demonstrated clock recovery/division from pseudo-data patterns at 20 Gb/s with various sub-frequency components using a semiconductor fiber ring laser. The clock recovery/division circuit is expected to find application in ultra high speed, OTDM networks either for demultiplexing, regeneration or data recovery. The circuit has been fully characterized and produces stable pulsetrains of 4.7 ps duration at 20 GHz and less than 3 ps at 10 and 5 GHz over a 16 nm tuning range across which output power and pulsewidth is almost constant. Especially for clock division, a weak sub-frequency component must be retained, around -32 dB lower than the line rate frequency component, in order to achieve a suppression ratio of more than 35 dB at the output signal.

Operation of the circuit can be extended in principle at least up to 40 GHz [13] using the same oscillator, when shorter input pulses are used in the

input data stream. To this end, using almost the same set-up, clock extraction at the data rate or at any of the sub-multiple of the data rate can be achieved. The parameters that are crucial for the extension of the operation and affect the formation of the mode-locked pulse at any repetition rate are the small signal gain and carrier lifetime of the SOA, the cavity loss and the energy/pulsewidth of the external pulses, as discussed in [14]. According to this analysis, in order to obtain the shortest pulses at all repetition rates, the aforementioned parameters must be adjusted so that the mode-locked pulse forms approximately half-way between two consecutive external pulses. Finally, operation to even higher rates requires the use of longer SOAs with higher gain and shorter recovery time.

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